HITACHI IC MEMORIES

HM4816A-3, HM4816A-4, HM4816A-7
HM4816AP-3, HM4816AP-4, HM4816AP-7

HITACHI

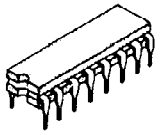
16384-word by 1-bit Dynamic Random Access Memory

The HM4816A is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816A (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power.

The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816A a truly superior RAM product. Multiplexed address inputs permits the HM4816A to be packaged in a standard 16-pin DIP.

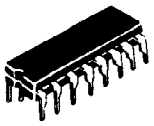
Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

HM4816A-3, HM4816A-4
HM4816A-7



(DG-16A)

HM4816AP-3, HM4816AP-4
HM4816AP-7



(DP-16)

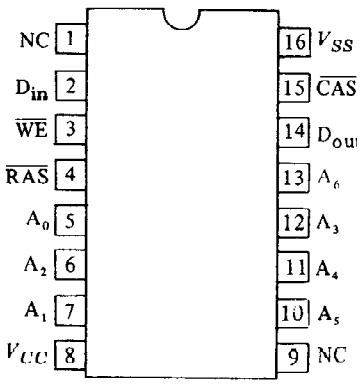
■ FEATURES

- Single 5V supply
  Low power standby and operation
  (Standby: 11mW max., operation: 150mW max.)
- Fast access time & cycle time

		HM4816A-3 HM4816AP-3	HM4816A-4 HM4816AP-4	HM4816A-7 HM4816AP-7
Maximum Access Time	(ns)	100	120	150
Read, Write Cycle	(ns)	235	270	320
Read-Modify-Write Cycle	(ns)	285	320	410

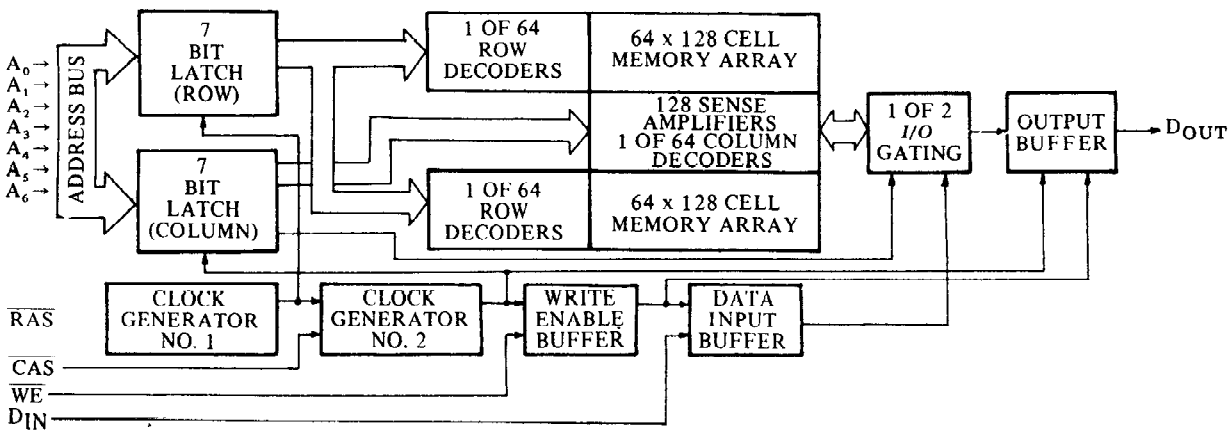
- Directly TTL compatible: All inputs & outputs
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "eary write" operation.
- Read modify write, $\overline{RAS}$ only refresh and page mode capability
- Only 128 refresh cycle required every 2ms
- Compatible with Intel 2118-3/-4/-7

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	HM4816A or AP	Unit
Voltage on any pin relative to GND		V_T	−1.0 ~ +7.0	V
Power supply voltage relative to GND		V_{CC}	−0.5 ~ +7.0	V
Short-circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	1.0	W
Operating Temperature		T_{opr}	0 ~ +70	°C
Storage Temperature	Cerdip	T_{stg}	−65 ~ +150	°C
	Plastic		−55 ~ +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Units	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1, 2
Input high (logic 1) voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IHC}	2.4	–	7.0	V	1
Input high (logic 1) voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}	2.4	–	7.0	V	1
Input low (logic 0) voltage all inputs	V_{IL}	−2.0	–	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

■ D.C. AND OPERATING CHARACTERISTICS[1]

(T_A =0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} =0V, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit	Notes
Input Load Current (any input)	$\lvert I_{LI} \rvert$	$V_{IN}=V_{SS}$ to V_{CC}	–	0.1	10	μA	
Output Leakage Current for High Impedance State	$\lvert I_{LO} \rvert$	Chip Deselected: $\overline{CAS}$ at V_{IH}. V_{OUT}=0 to 5.5V	–	0.1	10	μA	
V_{CC} Supply Current. Standby	I_{CC1}	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	–	1.2	2	mA	
V_{CC} Supply Current. Operating	I_{CC2}	HM4816A, AP-3 $t_{RC}=t_{RCMIN}$	–	23	27	mA	3
		HM4816A, AP-4 $t_{RC}=t_{RCMIN}$	–	21	25	mA	3
		HM4816A, AP-7 $t_{RC}=t_{RCMIN}$	–	19	23	mA	3
V_{CC} Supply Current: $\overline{RAS}$-Only Cycle	I_{CC3}	HM4816A, AP-3 $t_{RC}=t_{RCMIN}$	–	16	18	mA	3
		HM4816A, AP-4 $t_{RC}=t_{RCMIN}$	–	14	16	mA	3
		HM4816A, AP-7 $t_{RC}=t_{RCMIN}$	–	12	14	mA	3
V_{CC} Supply Current. Standby. Output Enabled	I_{CC5}	$\overline{CAS}$ at V_{IL}. $\overline{RAS}$ at V_{IH}	–	3	6	mA	3
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	–	–	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −5mA	2.4	–	–	V	

NOTES: 1. All voltages referenced to V_{SS}.
2. Typical values are for T_A = 25° C and nominal supply voltages.
3. I_{CC} is dependent on output loading when the devices output is selected. Specified I_{CC} MAX is measured with the output open.

■ CAPACITANCE[1]

(T_A=25°C, V_{CC}=5V ±10%, V_{SS}=0V, unless otherwise noted.)

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address. Data In	3	5	pF
C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, Data Out	4	7	pF

Notes: : 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C=\frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

■ A.C. CHARACTERISTICS [1.2.3]

(T_A =0°C to 70°C. V_{CC}=5V ±10%. V_{SS}=0V. unless otherwise noted.)

• READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	HM4816A-3 HM4816AP-3		HM4816A-4 HM4816AP-4		HM4816A-7 HM4816AP-7		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time From $\overline{RAS}$	–	100	–	120	–	150	ns	4.5
t_{CAC}	Access Time From $\overline{CAS}$	–	55	–	65	–	80	ns	4.5.6
t_{REF}	Time Between Refresh	–	2	–	2	–	2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	110	–	120	–	135	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (non-page cycles)	50	–	55	–	70	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	45	25	55	25	70	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	70	–	85	–	105	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	165	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	20	–	ns	
t_{AR}	Column Address Hold Time to $\overline{RAS}$	60	–	75	–	90	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	45	0	50	0	60	ns	

• READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	235	–	270	–	320	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10000	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	55	10000	65	10000	95	10000	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	10	–	10	–	10	–	ns	

• WRITE CYCLE

t_{RC}	Random Write Cycle Time	235	–	270	–	320	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10000	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	55	10000	65	10000	95	10000	ns	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	9
t_{WCH}	Write Command Hold Time	25	–	30	–	45	–	ns	
t_{WCR}	Write Command Hold Time to $\overline{RAS}$	70	–	85	–	115	–	ns	
t_{WP}	Write Command Pulse Width	25	–	30	–	50	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60	–	65	–	110	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	45	–	50	–	100	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	
t_{DH}	Data-In Hold Time	25	–	30	–	45	–	ns	
t_{DHR}	Data-In Hold Time to $\overline{RAS}$	70	–	85	–	115	–	ns	

• READ-MODIFY-WRITE CYCLE

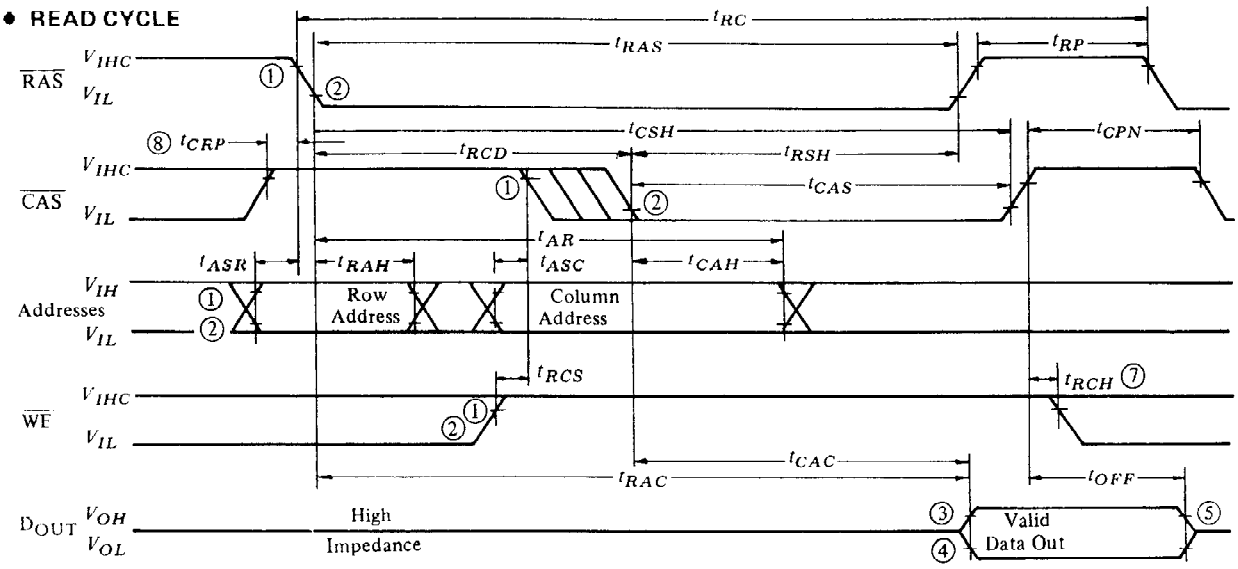
t_{RWC}	Read-Modify-Write Cycle Time	285	–	320	–	410	–	ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	165	10000	190	10000	265	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	105	10000	120	10000	185	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100	–	120	–	150	–	ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	55	–	65	–	80	–	ns	9

Notes:

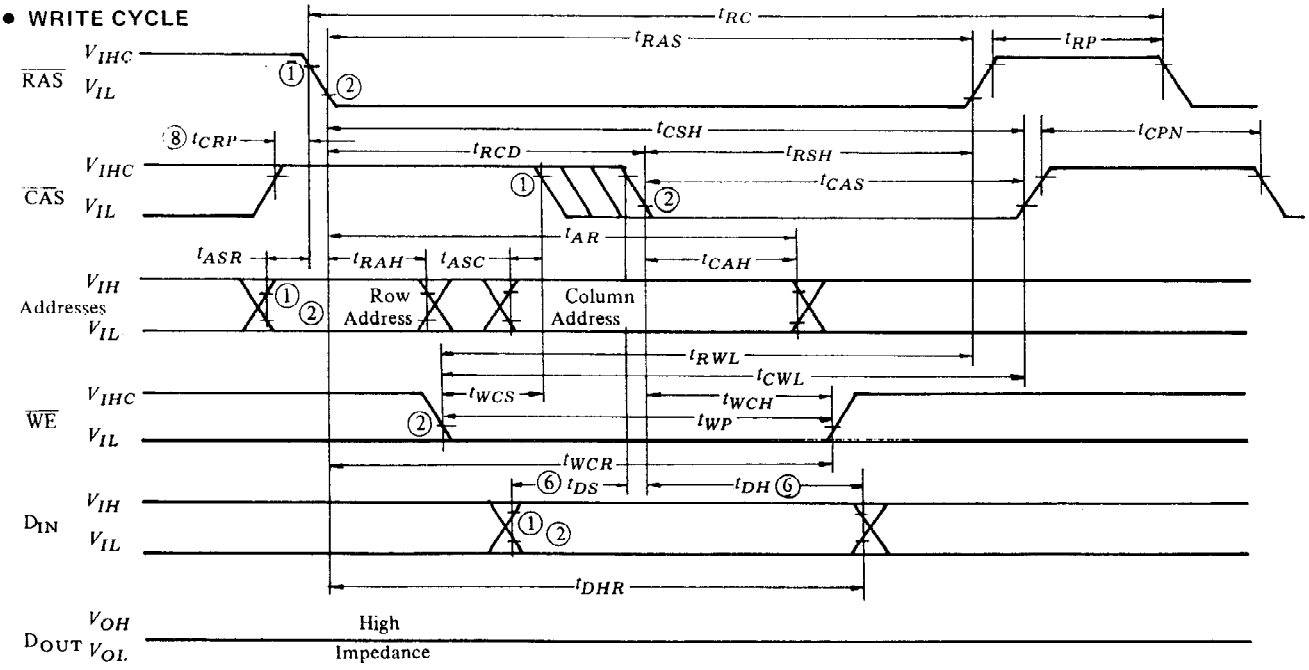
1. All voltages referenced to V_{SS}
2. Eight cycles are required atter power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. AC Characteristics assume t_T=5ns
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.) If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.)
5. Load = 2 TTL loads and 100pF
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.)
7. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.)
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address if neither of the above conditions is satisfied, the condition on the data out is indeterminate.

■ WAVEFORMS

◆ READ CYCLE



● WRITE CYCLE



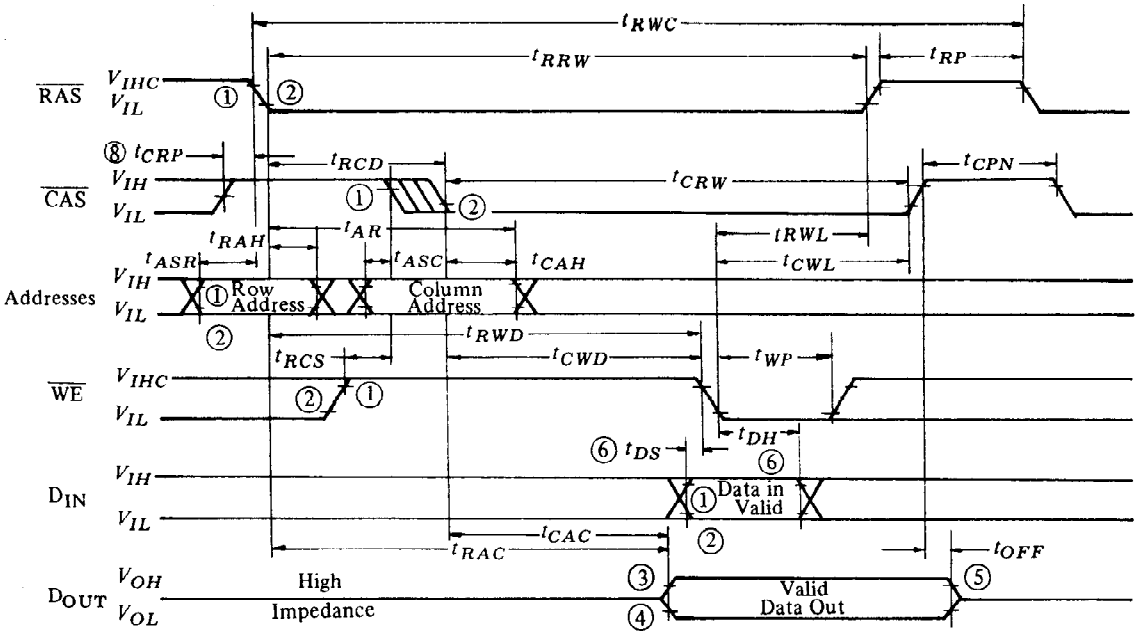
Notes:

1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

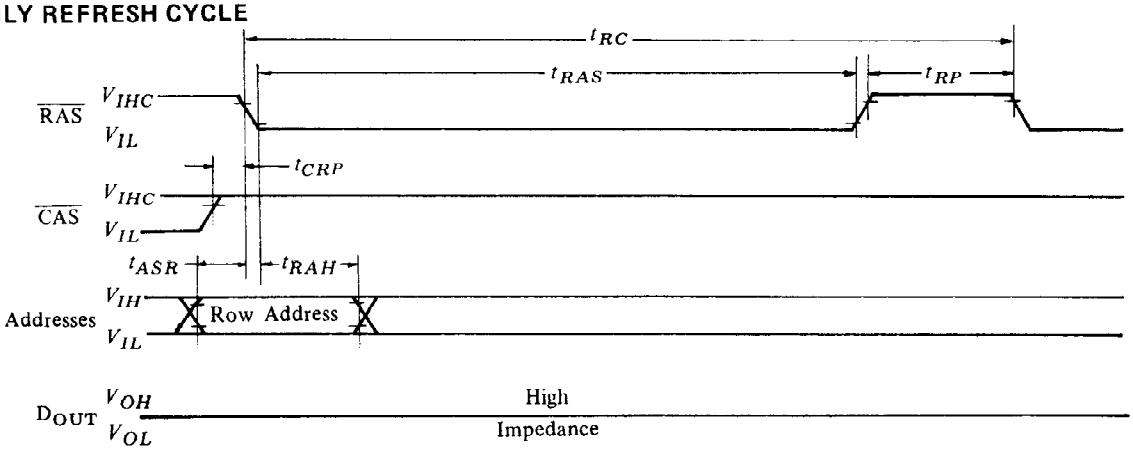
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} if measured to $I_{OUT} < |I_{LO}|$.
6. t_{OS} and t_{OH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
8. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

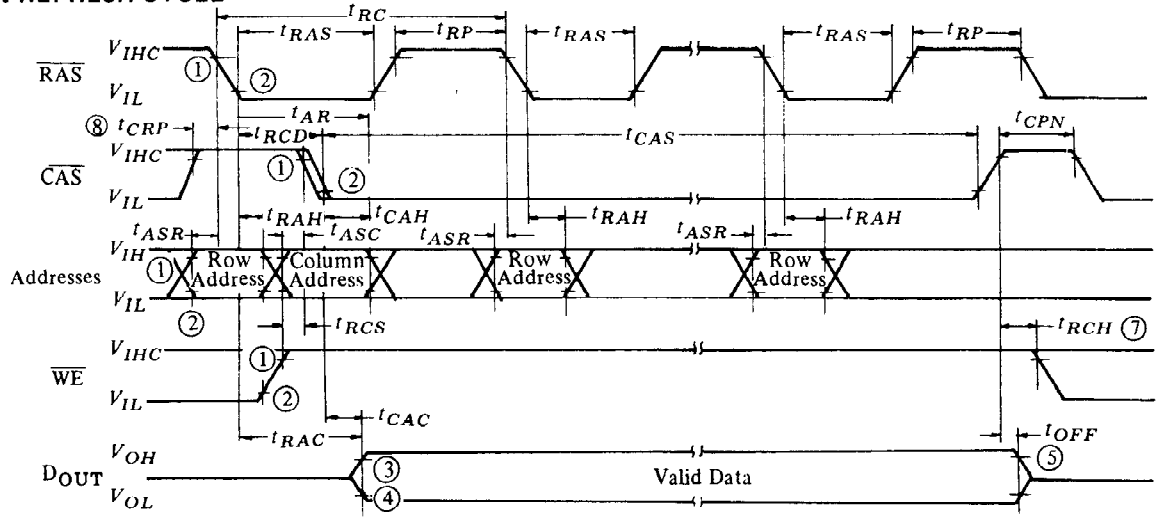
• READ-MODIFY-WRITE CYCLE



• RAS-ONLY REFRESH CYCLE



• HIDDEN REFRESH CYCLE



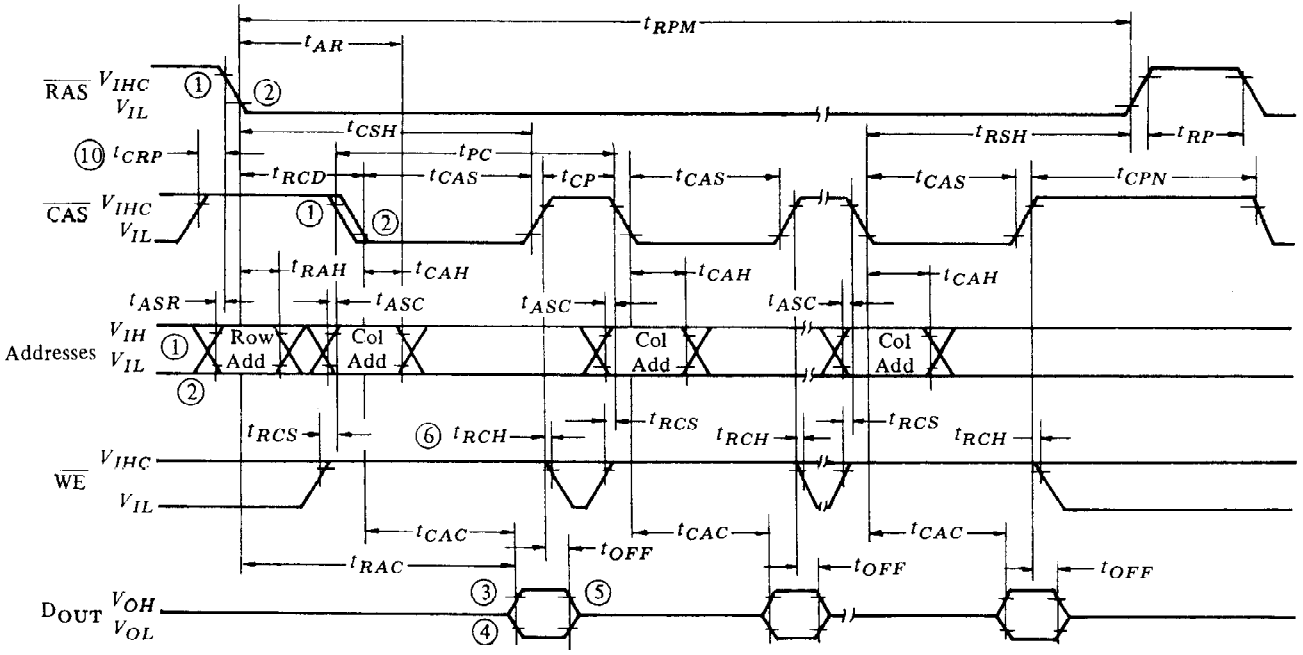
Notes: 1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ and reference levels for measuring timing of input signals.
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} < |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
8. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

■ D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7.8.]

(T_A =0°C to 70°C, V_{CC}=5V ±10%, V_{SS}=0V, unless otherwise noted.)

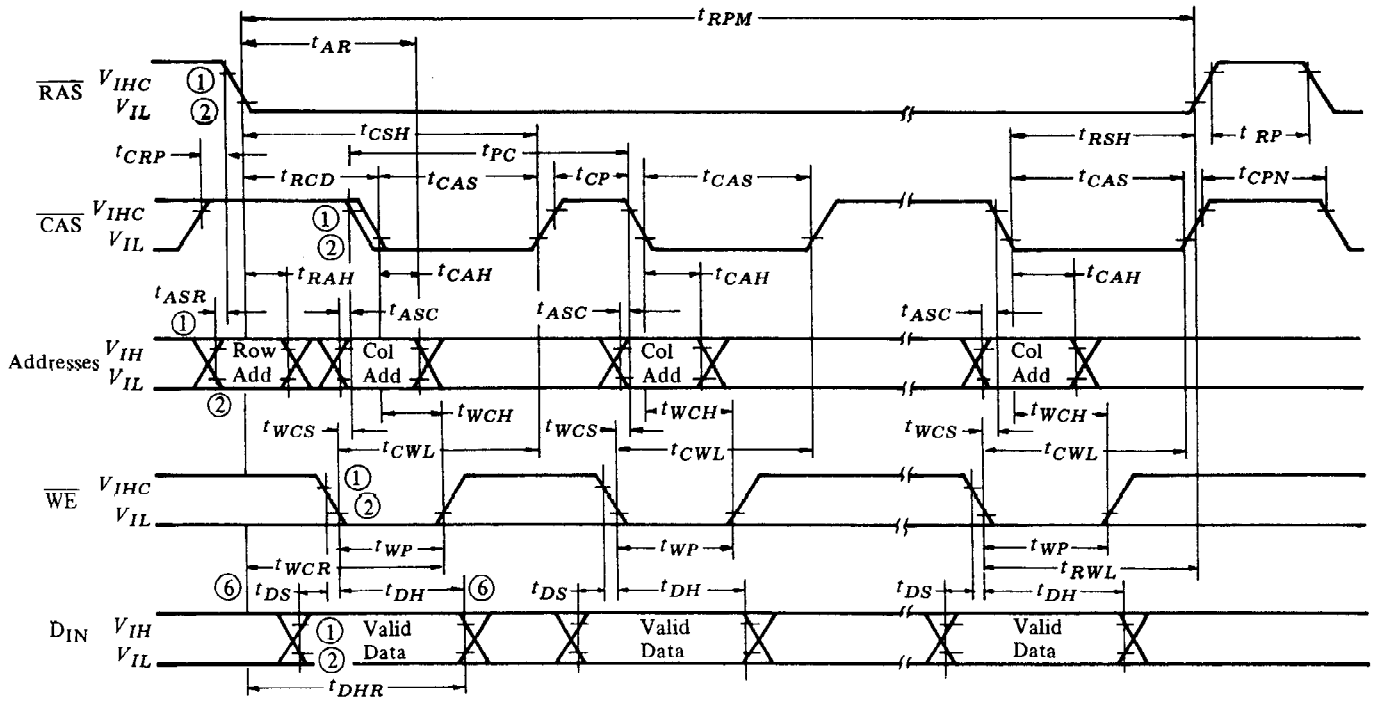
Symbol	Parameter	HM4816A-3 HM4816AP-3		HM4816A-4 HM4816AP-4		HM4816A-7 HM4816AP-7		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PC}	Page Mode Read or Write Cycle	125	–	145	–	190	–	ns
t_{PCM}	Page Mode Read Modify Write Cycle	175	–	200	–	280	–	ns
t_{CP}	$\overline{CAS}$ Precharge Time. Page Cycle	60	–	70	–	85	–	ns
t_{RPM}	$\overline{RAS}$ Pulse Width. Page Mode	115	10000	140	10000	175	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	55	10000	65	10000	95	10000	ns
I_{DD4}	V_{DD} Supply Current Page Mode. Minimum t_{PC}. Minimum t_{CAS}	–	23	–	21	–	18	mA

● PAGE MODE READ CYCLE

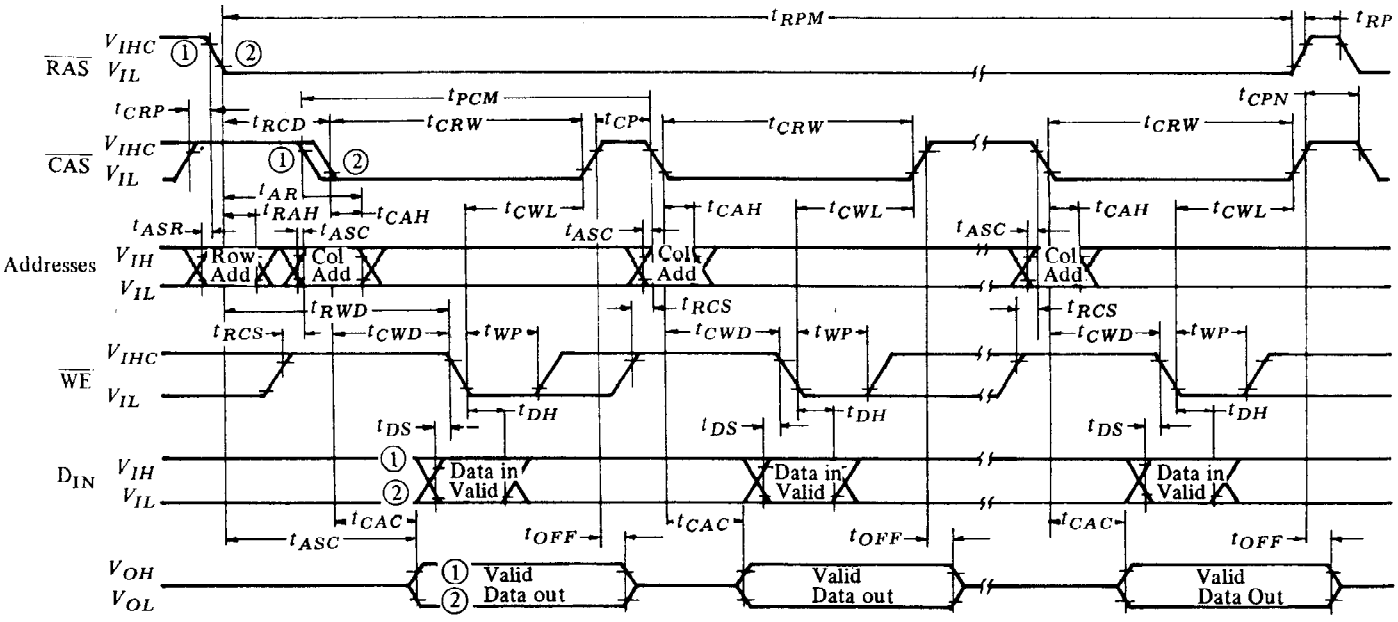


Notes:
1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} < |I_{LO}|$.
6. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$,whichever occurs first.
7. All voltages referenced to V_{SS}.
8. AC Characteristic assume t_T=5ns.
9. See the typical characteristics section for values of this parameter under alternate conditions.
10. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
11. All previously specified A.C. and D.C. characteristics are applicable to their respective page mode device.

• PAGE MODE WRITE CYCLE

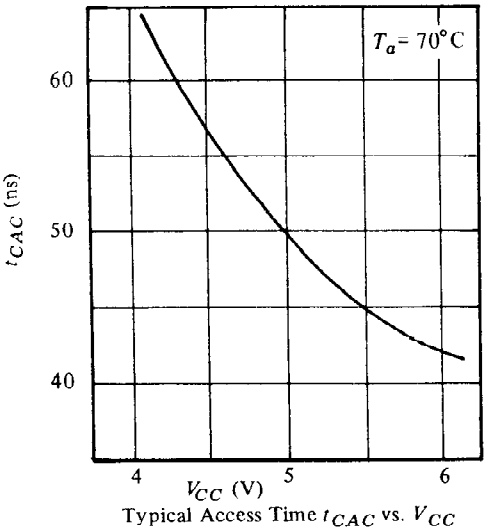


• PAGE MODE READ-MODIFY-WRITE CYCLE

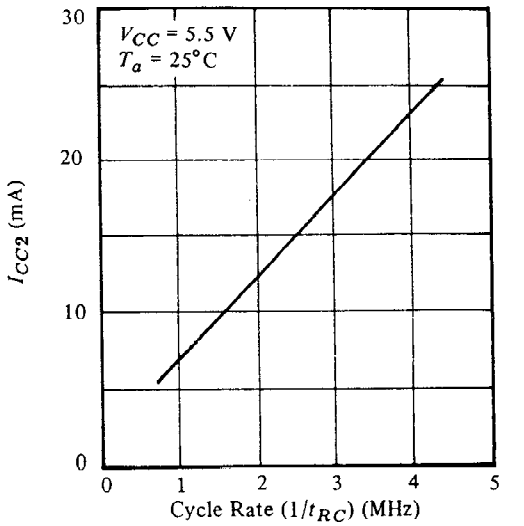


Notes: 1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $|I_{OUT}| < |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
8. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

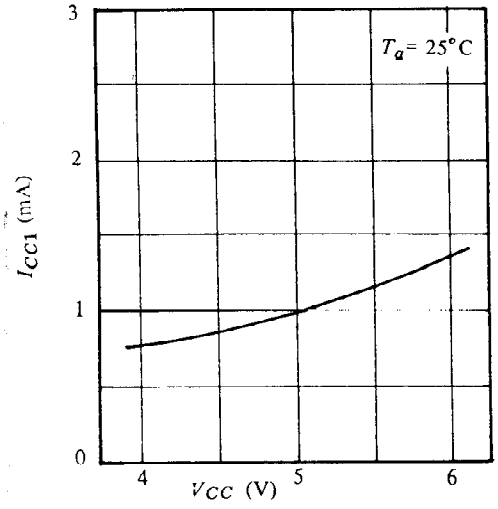
Typicl Characteristics of HM4816A



Typical Access Time t_{CAC} vs. V_{CC}

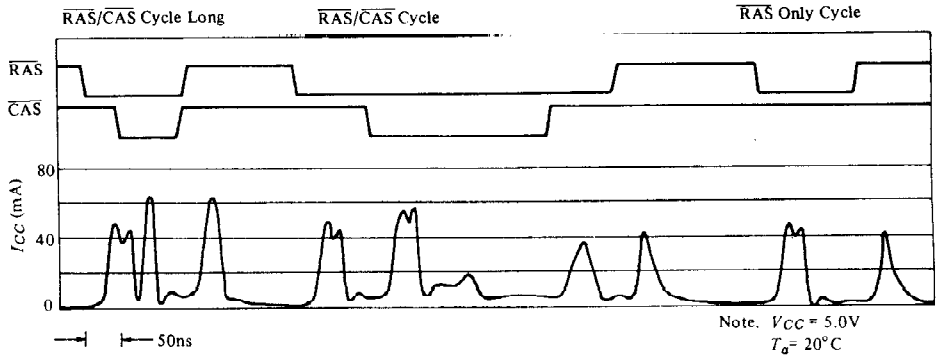


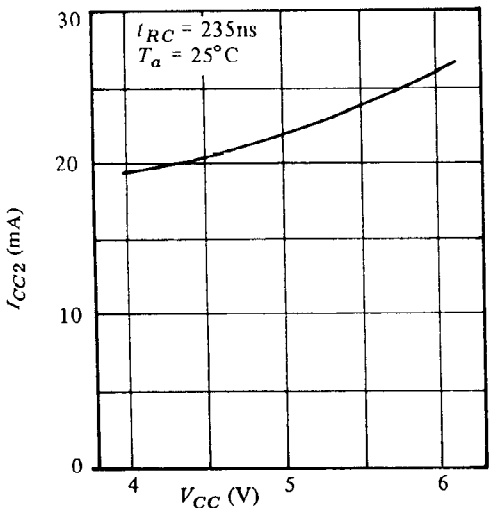
Typical Operating Current I_{CC2} vs. Cycle Rate.



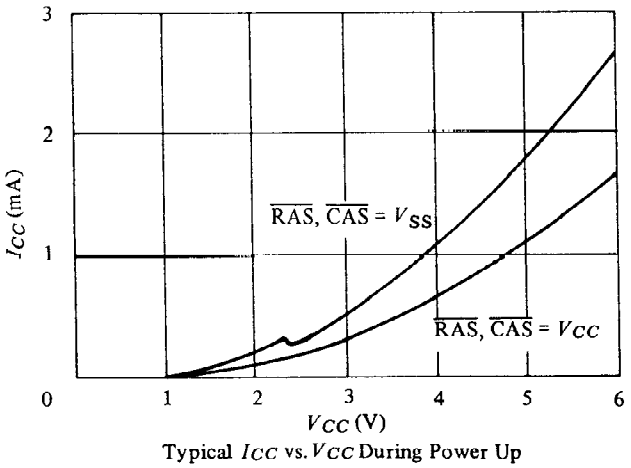
Typical Standby Current I_{CC1} vs. V_{CC}

• TYPICAL SUPPLY CURRENT WAVEFORMS





Typical Operating Current I_{CC2} vs. V_{CC}



Typical I_{CC} vs. V_{CC} During Power Up