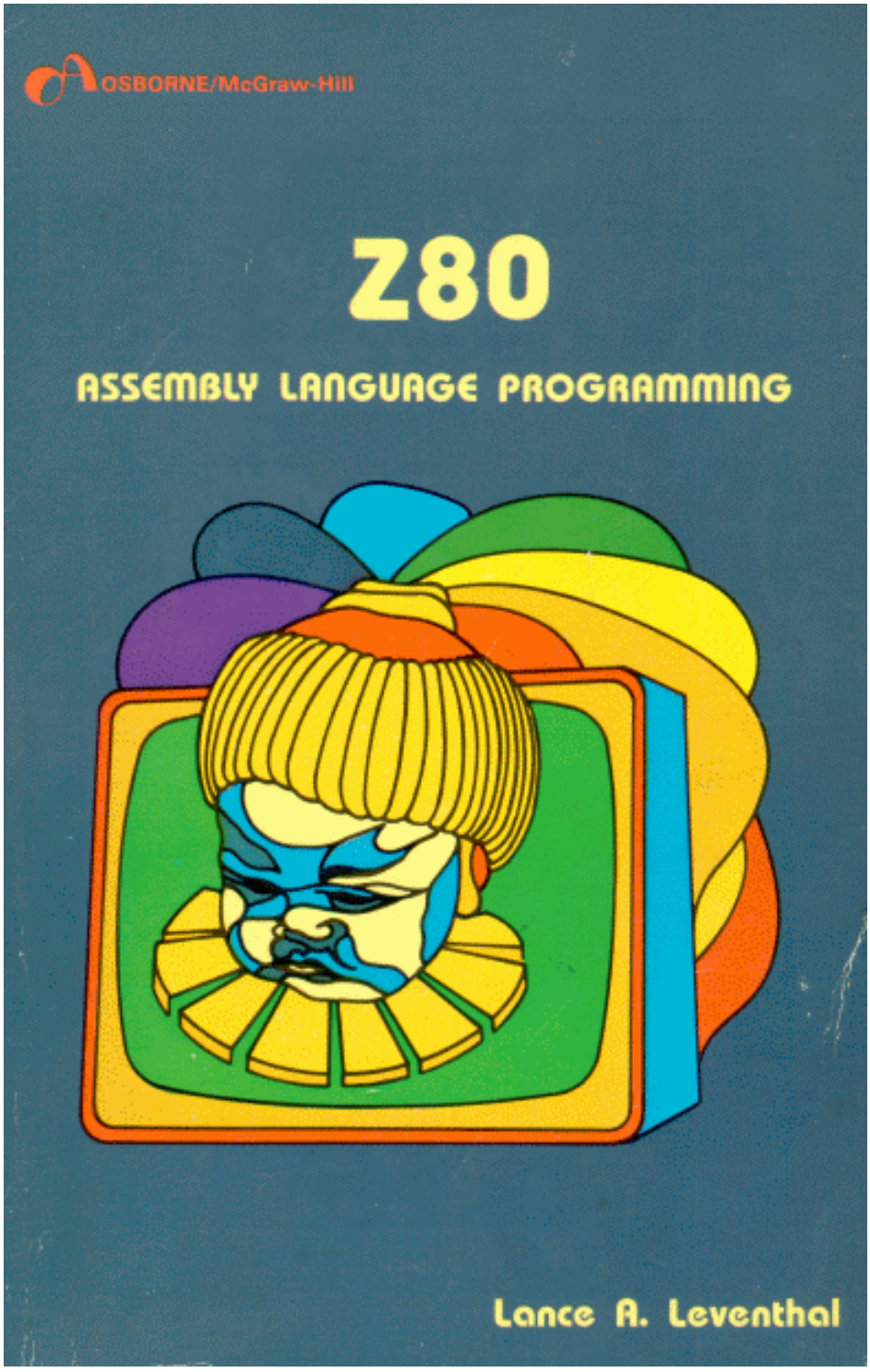

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8080A/Z80 compatability

8080A/Z80 COMPATIBILITY

8080A/Z80 COMPATIBILITY FEATURES

Although the Z80 microprocessor can certainly be used on its own merits, one of its important characteristics is its compatibility with the 8080A microprocessor. This compatibility has the following features:

1) All 8080A machine language instructions are also Z80 machine language instructions.
2) All 8080A registers are also Z80 registers (see Table 3-6).
3) Almost all 8080A programs will run on a Z80, with some minor differences to be noted later.
4) The Z80 has instructions, registers, and other features not present on the 8080A, so Z80 programs will not generally run on 8080A processors.

8080A/Z80 ASSEMBLY LEVEL CONVERSION

Note that this compatibility does not extend to assembly language source statements since Z80 assemblers and 8080A assemblers use different operation code mnemonics. **Table 3-7 contains a list of the 8080A mnemonic codes and the corresponding Z80 codes, while Table 3-8 is the same list organized by Z80 codes.**

8080A UNUSED OPERATION CODES

Readers should note the binary coding limitations that this compatibility places on the extra features of the Z80 microprocessor. The 8080A has some unused operation codes (see Table 3-9) that are used for some of the Z80's extra instructions. But there are simply not enough such codes to cover the large number of features in a simple form.

2-BYTE OPERATION CODES

Thus, many of the added Z80 instructions require a 2-byte operation code. The first byte is CB, DD, ED, or FD. Note the following meanings of these codes from Table 3-9:

CB — a register or bit operation
DD — an operation involving register IX
ED — a miscellaneous non-8080A instruction not covered elsewhere
FD — an operation involving register IY

The second byte of the operation code describes the actual operation to be performed.

FASTER AND SLOWER EXECUTING INSTRUCTIONS

The end result is that these multi-byte instructions execute rather slowly (and use more memory) because an additional memory access is required. The reader should be aware of this variation in execution times and try to use faster executing instructions when possible. This warning particularly applies to the extra shift instructions (RLC, RRC, RL, RR, SRA, SRL) and to instructions involving the index registers IX and IY.

8080A/Z80 INCOMPATIBILITIES

There are a few minor incompatibilities between the 8080A and the Z80. These are:

1) The Z80 uses the P (or P/O) flag to indicate twos complement overflow after arithmetic operations. The 8080A always uses this flag for parity.
2) The Z80 and 8080A execute the DAA instruction differently. On the Z80, this instruction will correct decimal subtraction as well as decimal addition. On the 8080A, it will correct only decimal addition.
3) The Z80 rotate instructions clear the A_C flag. The 8080A rotate instructions do not affect the A_C flag.

Table 3-6. Register and Flag Correspondence between Z80 and 8080A

Z80 Register	8080A Register
A	A
A'	None
B	B
B'	None
C	C
C'	None
D	D
D'	None
E	E
E'	None
F	Least Significant Half of PSW
F'	None
H	H
H'	None
I	None
IX	None
IY	None
L	L
L'	None
R	None
PC	PC
SP	SP
Z80 Register Pairs	**8080A Register Pairs**
BC	B
DE	D
HL	H
AF	PSW
Z80 Flags	**8080A Flags**
C (Carry)	C (Carry)
H (Half-Carry)	AC (Auxiliary Carry)
N (Subtract)	None
P/O (Parity/Overflow)	P (Parity)
S (Sign)	S (Sign)
Z (Zero)	Z (Zero)

8085/Z80 INCOMPATIBILITIES

The Z80 is not compatible with the extra features of the 8085 microprocessor. The codes used for RIM and SIM on the 8085 are used for relative jumps (NZ and NC) on the Z80.

TIMING INCOMPATIBILITIES

Instruction timings on the 8080A, 8085, and Z80 all differ. Programs that depend on precise instruction timings will therefore execute properly only on the processor for which they were written.

The N flag on the Z80 occupies bit 2 of the F register; the corresponding bit in the Processor Status Word of the 8080A is always a logic '1'.

Table 3-7 Correspondence between 8080A and Z80 Mnemonics

8080A Mnemonic		Z80 Mnemonic	
ACI	data	ADC	A,data
ADC	reg or M	ADC	A,reg or (HL)
ADD	reg or M	ADD	A,reg or (HL)
ADI	data	ADD	A,data
ANA	reg or M	AND	reg or (HL)
ANI	data	AND	data
CALL	addr	CALL	addr
CC	addr	CALL	C,addr
CM	addr	CALL	M,addr
CMA		CPL	
CMC		CCF	
CMP	reg or M	CP	reg or (HL)
CNC	addr	CALL	NC,addr
CNZ	addr	CALL	NZ,addr
CP	addr	CALL	P,addr
CPE	addr	CALL	PE,addr
CPI	data	CP	data
CPO	addr	CALL	PO,addr
CZ	addr	CALL	Z,addr
DAA		DAA	
DAD	rp	ADD	HL,rp
DCR	reg or M	DEC	reg or (HL)
DCX	rp	DEC	rp
DI		DI	
EI		EI	
HLT		HALT	
IN	port	IN	A,(port)
INR	reg or M	INC	reg or (HL)
INX	rp	INC	rp
JC	addr	JP	C,addr
JM	addr	JP	M,addr
JMP	addr	JP	addr
JNC	addr	JP	NC,addr
JP	addr	JP	P,addr
JNZ	addr	JP	NZ,addr
JPE	addr	JP	PE,addr
JPO	addr	JP	PO,addr
JZ	addr	JP	Z,addr
LDA	addr	LD	A,(addr)
LDAX	B or D	LD	A,(BC) or (DE)

8080A Mnemonic		Z80 Mnemonic	
LHLD	addr	LD	HL,(addr)
LXI	rp,data16	LD	rp,data16
MOV	reg,reg or M	LD	reg,reg or (HL)
MOV	reg or M,reg	LD	reg or (HL),reg
MVI	reg or M,data	LD	reg or (HL),data
NOP		NOP	
ORA	reg or M	OR	reg or (HL)
ORI	data	OR	data
OUT	port	OUT	(port),A
PCHL		JP	(HL)
POP	pr	POP	pr
PUSH	pr	PUSH	pr
RAL		RLA	
RAR		RRA	
RC		RET	C
RET		RET	
RLC		RLCA	
RM		RET	M
RNC		RET	NC
RNZ		RET	NZ
RP		RET	P
RPE		RET	PE
RPO		RET	PO
RRC		RRCA	
RST	n	RST	n
RZ		RET	Z
SBB	reg or M	SBC	A,reg or (HL)
SBI	data	SBC	A,data
SHLD	addr	LD	(addr),HL
SPHL		LD	SP,HL
STA	addr	LD	(addr),A
STAX	B or D	LD	(BC) or (DE),A
STC		SCF	
SUB	reg or M	SUB	reg or (HL)
SUI	data	SUB	data
XCHG		EX	DE,HL
XRA	reg or M	XOR	reg or (HL)
XRI	data	XOR	data
XTHL		EX	(SP),HL

Table 3-8. Correspondence between Z80 and 8080A Mnemonics

Z80 Mnemonic		8080A Mnemonic	
ADC	A,data	ACI	data
ADC	A,(HL)	ADC	M
ADC	A,reg	ADC	reg
ADC	A,(xy + disp)	—	
ADC	HL,rp	—	
ADD	A,data	ADI	data
ADD	A,(HL)	ADD	M
ADD	A,reg	ADD	reg
ADD	A,(xy + disp)	—	
ADD	HL,rp	DAD	rp
ADD	IX,pp	—	
ADD	IY,rr	—	
AND	data	ANI	data
AND	(HL)	ANA	M
AND	reg	ANA	reg
AND	(xy + disp)	—	
BIT	b,(HL)	—	
BIT	b,reg	—	
BIT	b,(xy + disp)	—	
CALL	addr	CALL	addr
CALL	C,addr	CC	addr
CALL	M,addr	CM	addr
CALL	NC,addr	CNC	addr
CALL	NZ,addr	CNZ	addr
CALL	P,addr	CP	addr
CALL	PE,addr	CPE	addr
CALL	PO,addr	CPO	addr
CALL	Z,addr	CZ	addr
CCF		CMC	
CP	data	CPI	data
CP	(HL)	CMP	M
CP	reg	CMP	reg
CP	(xy + disp)	—	
CPD		—	
CPDR		—	
CPI		—	
CPIR		—	
CPL		CMA	
DAA		DAA	
DEC	(HL)	DCR	M
DEC	reg	DCR	reg
DEC	rp	DCX	rp
DEC	xy	—	
DEC	(xy + disp)	—	
DI		DI	
DJNZ	disp	—	
EI		EI	
EX	AF,AF'	—	
EX	DE,HL	XCHG	
EX	(SP),HL	XTHL	
EX	(SP),xy	—	
EXX		—	
HALT		HLT	
IM	m	—	
IN	A,(port)	IN	port
IN	reg,(C)	—	
INC	(HL)	INR	M
INC	reg	INR	reg

Z80 Mnemonic		8080A Mnemonic	
INC	rp	INX	rp
INC	xy	—	
INC	(xy + disp)	—	
IND		—	
INDR		—	
INI		—	
INIR		—	
JP	addr	JMP	addr
JP	C,addr	JC	addr
JP	(HL)	PCHL	
JP	M,addr	JM	addr
JP	NC,addr	JNC	addr
JP	NZ,addr	JNZ	addr
JP	P,addr	JP	addr
JP	PE,addr	JPE	addr
JP	PO,addr	JPO	addr
JP	Z,addr	JZ	addr
JP	xy	—	
JR	C,disp	—	
JR	disp	—	
JR	NC,disp	—	
JR	NZ,disp	—	
JR	Z,disp	—	
LD	A,(addr)	LDA	addr
LD	A,(BC) or (DE)	LDAX	B or D
LD	A,I	—	
LD	A,R	—	
LD	(addr),A	STA	addr
LD	(addr),BC or DE	—	
LD	(addr),HL	SHLD	addr
LD	(addr),SP	—	
LD	(addr),xy	—	
LD	(BC) or (DE),A	STAX	B or D
LD	BC or DE,(addr)	—	
LD	HL,(addr)	LHLD	addr
LD	(HL),data	MVI	M,data
LD	(HL),reg	MOV	M,reg
LD	I,A	—	
LD	R,A	—	
LD	reg,data	MVI	reg,data
LD	reg,(HL)	MOV	reg,M
LD	reg,reg	MOV	reg,reg
LD	reg,(xy + disp)	—	
LD	rp,data16	LXI	rp,data16
LD	SP,(addr)	—	
LD	SP,HL	SPHL	
LD	SP,xy	—	
LD	xy,data16	—	
LD	xy,(addr)	—	
LD	(xy + disp),data	—	
LD	(xy + disp),reg	—	
LDD		—	
LDDR		—	
LDI		—	
LDIR		—	
NEG		—	
NOP		NOP	
OR	data	ORI	data

— indicates that there is no corresponding instruction.

Table 3-8. Correspondence between Z80 and 8080A Mnemonics (Continued)

Z80 Mnemonic		8080A Mnemonic	
OR	(HL)	ORA	M
OR	reg	ORA	reg
OR	(xy + disp)	—	
OTDR		—	
OTIR		—	
OUT	(C),reg	—	
OUT	(port),A	OUT	port
OUTD		—	
OUTI		—	
POP	pr	POP	pr
POP	xy	—	
PUSH	pr	PUSH	pr
PUSH	xy	—	
RES	b,(HL)	—	
RES	b,reg	—	
RES	b,(xy + disp)	—	
RET		RET	
RET	C	RC	
RET	M	RM	
RET	NC	RNC	
RET	NZ	RNZ	
RET	P	RP	
RET	PE	RPE	
RET	PO	RPO	
RET	Z	RZ	
RETI		—	
RETN		—	
RL	(HL)	—	
RL	reg	—	
RL	(xy + disp)	—	
RLA		RAL	
RLC	(HL)	—	
RLC	reg	—	
RLC	(xy + disp)	—	
RLCA		RLC	
RLD		—	

Z80 Mnemonic		8080A Mnemonic	
RR	(HL)	—	
RR	reg	—	
RR	(xy + disp)	—	
RRA		RAR	
RRC	(HL)	—	
RRC	reg	—	
RRC	(xy + disp)	—	
RRCA		RRC	
RRD		—	
RST	n	RST	n
SBC	A,data	SBI	data
SBC	A,(HL)	SBB	M
SBC	A,reg	SBB	reg
SBC	A,(xy + disp)	—	
SBC	HL,rp	—	
SCF		STC	
SET	b,(HL)	—	
SET	b,reg	—	
SET	b,(xy + disp)	—	
SLA	(HL)	—	
SLA	reg	—	
SLA	(xy + disp)	—	
SRA	(HL)	—	
SRA	reg	—	
SRA	(xy + disp)	—	
SRL	(HL)	—	
SRL	reg	—	
SRL	(xy + disp)	—	
SUB	data	SUI	data
SUB	(HL)	SUB	M
SUB	reg	SUB	reg
SUB	(xy + disp)	—	
XOR	data	XRI	data
XOR	(HL)	XRA	M
XOR	reg	XRA	reg
XOR	(xy + disp)	—	

— indicates that there is no corresponding instruction

Table 3-9. Unused 8080A Operation Codes and Their Z80 Meanings

8080A Operation Code	Z80 Use
08	EX AF,AF'
10	DJNZ disp
18	JR disp
20 (RIM on 8085)	JR NZ,disp
28	JR Z,disp
30 (SIM on 8085)	JR NC,disp
38	JR C,disp
CB	BIT, RES, RL, RLC, RR, RRC, SET, SLA, SRA, SRL
D9	EXX
DD	All instructions involving Register IX.

ED	ADC HL,rp
	CPD
	CPDR
	CPI
	CPIR
	IM m
	IN reg,(C)
	IND
	INDR
	INI
	INIR
	LD A,I
	LD A,R
	LD (addr),rp
	LD I,A
	LD R,A
	LD rp,(addr)
	LDD
	LDDR
	LDI
	LDIR
	NEG
	OTDR
	OTIR
	OUT (C),reg
	OUTD
	OUTI
	RETI
	RETN
	RLD
	RRD
	SBC HL,rp

FD	All instructions involving Register IY.